

PTO-1449		Application No. Unknown 10/722 930		Applicant(s) Prasun K. Raha	
Information Disclosure Citation In an Application		Docket Number TI-37052 (032350.B543)		Group Art Unit Unknown	
				Filing Date November 25, 2003	

U.S. PATENT DOCUMENTS						
	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
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FOREIGN PATENT DOCUMENTS							
	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
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		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
R	f4	Hiok-Tiaq Ng and David J. Allstot, CMOS Current Steering Logic for Low-Voltage Mixed-Signal Integrated Circuits, IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 5, No. 3, pages 301-308.	September 1997
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EXAMINER LUU	DATE CONSIDERED 4/26/05
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<p>Substitute for Form 1449A/PTO</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p> <p>(use as many sheets as necessary)</p>			Complete If Known	
			Application Number	10/722,930
			Filing Date	11/25/03
			First Named Inventor	Prasun K. Raha
			Group Art Unit	2847 2816
Examiner Name	TBD			
Sheet 1 of 1	Attorney Docket No.		TI-37052	

U.S. PATENT DOCUMENTS						
Exam. Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
AK	AA	5,635,878		Liu et al.	6/3/97	
AK	AB	5,420,547		Kikuchi	5/30/95	
	AC					
	AD					
	AE					
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS					
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AK	CA	KATAKURA MASAYUKI, Patent Abstracts of Japan, Vol. 1998, No. 01, January 30, 1998, JP 09246922, Publication Date 9/19/97			
JN	CB	KUROOKA KAZUAKI, Patent Abstracts of Japan, Vol. 2000, No. 23, February 10, 2001, JP 2001156600, Publication Date 6/8/01			
	CC				
	CD				
	CE				
	CF				
	CG				

Examiner Signature	LULU	Date Considered	5/16/05
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